REMARKS

Claims 1-20 are pending in the Application.

Claims 1-20 stand rejected.

Claim 7 stands objected to.

I. OBJECTED TO CLAIM

Claim 7 has been objected to in the summary of the action. The detailed action inadvertently omitted the basis for the objection. The Applicant's attorney and Examiner Li discussed this in a telephonic interview on November 25, 2003, and Examiner Li noted that the clause "with the" was repeated twice in succession in line 2 of claim 7. Accordingly, claim 7 has been rewritten hereinabove to correct the informality, and the Applicant respectfully requests that the objection to claim 7 be withdrawn.

II. REJECTION UNDER 35 U.S.C. § 103

Claims 1-20 have been rejected under 35 U.S.C. § 103 as being unpatentable over *Horton et al.*, U.S. Patent No. 6,223,280 ("*Horton*") in view of *Rahman et al.*, U.S. Patent No. 5,805,878 ("*Rahman*"). The Applicant respectfully traverses the rejections of claims 1-20 under 35 U.S.C. § 103.

Claim 1 is directed to a method of generating a global history vector. The method includes determining if a selected group of instructions contains a branch instruction. The method further includes:

maintaining a current global history vector in a shift register when the selected group does not contain a branch instruction;

shifting a first value into the shift register to generate a second vector if the selected group contains a branch instruction and the branch instruction is predicted as a branch taken; and

shifting a second value into the shift register to generate a second vector when

the selected group contains a branch instruction and the selected group does not include a branch instruction predicted as a branch taken.

Claim 1 has been rejected on the ground that *Horton* teaches, *inter alia*, determining if a branch instruction is present. (Paper No. 3, page 3.) As an initial matter, this assertion does not address the limitation in claim 1 reciting the step of determining if a selected group of instructions contains a branch instruction. All words in the claim must be considered when determining the patentability of the claim. MPEP § 2143.02. *Horton* is directed to systems for preloading a branch prediction circuit with data. (*Horton*, col. 1, lines 1-10.) The teaching referred to states in substance that a branch prediction unit is preloaded with data which may be a multibit predictor, and wherein the data is preloaded by the microprocessor in response to an instruction for preloading the predetermined data. (*See Horton*, col. 8, lines 34-49.) This does not discuss determining if a branch instruction is present.

With respect to the limitation in claim 1 directed to maintaining a current global history vector in a shift register if the selected group does not contain a branch instruction, the Examiner refers to the same teaching in *Horton* discussed above. This teaching does not disclose or suggest this limitation of claim 1. *Horton* is also stated to teach that branch prediction elements are changed when a branch is detected, but no reference in *Horton* is cited. Paper No. 3, page 3.) Nonetheless, this limitation of claim 1 does not recite that branch prediction elements are changed when a branch is detected.

With respect to the limitations reciting the steps of shifting first and second values into the shift register... , the Examiner cites to several teachings in *Horton.* (Paper No. 3, page 3) (citing *Horton*, Abstract; col. 2, line 43 to col. 3, line 14; col. 8, line 63 to col. 9, line 16; FIGURES 2, 3 and 4). The Abstract discusses, in substance, loading a branch history shift register with a predetermined multibit predictor in response to the microprocessor receiving a special write history instruction. (*Horton*, Abstract.) Once the branch history storage device is preloaded, the prediction circuits predict the results of a conditional branch instruction using the predetermined multibit predictor after the conditional branch instruction is received by the microprocessor

but before it is executed. (*Id.*) The Examiner also relies on teaching in *Horton* that generally discusses branch prediction techniques, and which plainly do not disclose the aforementioned limitations of claim 1. (*See Horton*, col. 2, line 43 through col. 3, line 14) (discussing various branch prediction mechanisms such as static or dynamic, local or global etc.) Lastly, the Examiner relies on teaching that discloses that the branch history shift register holds either the predetermined multibit predictor, or the contents of the checkpoint register, depending on whether a write history register signal is received (as a consequence of the execution of a write history register instruction). (*Horton*, col. 8, line 63 through col. 9, line 15.) This is also seen in block 41 (MUX) of FIGURE 2, and steps 60 and 62 of FIGURE 3, and step 86 of FIGURE 4. (*Horton*, FIGURES 2, 3 and 4.) These do not show the aforesaid limitations of claim 1. Furthermore, FIGURE 4 shows that a prediction is shifted into the branch history shift register in response to a prediction request. It does not show respectively shifting first and second values into a history shift register when the selected group contains a branch instruction that is predicted taken, and when the selected group contains a branch instruction not including a branch instruction predicted as taken.

The Examiner admits that Horton does not teach fetching a selected group of instructions. (Paper No. 3, page 3.) *Rahman* is asserted to supply the admittedly missing teaching. (Paper No. 3, page 3) (citing *Rahman*, col. 4, lines 42-61.) Whether *Rahman* teaches fetching a selected group of instructions, or not, it does not cure *Horton*. *Rahman* does not supply the limitations of claim 1 that are missing from *Horton* as discussed above. Indeed, the Examiner does not contend that either *Horton* or *Rahman* teach determining if a selected group of instructions contains a branch instruction. (*See* Paper No. 3, page 3.)

Consequently, for at least the aforesaid reasons, neither *Horton* nor *Rahman* alone or in combination teach or suggest the limitations of claim 1.

The Examiner also asserts that it would have been obvious to combine the references because fetching a group of instructions from a cache to improve performance of the processor. However, this assertion does not address the invention

of claim 1. Furthermore, a motivation or suggestion to combine references must be clear and particular, and broad conclusory statements regarding the teachings standing alone are not evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1616-17 (Fed. Cir. 1999).

Thus, for at least the aforesaid reasons, a *prima facie* showing of obviousness has not been made for claim 1. Therefore, claim 1 is allowable under 35 U.S.C. § 103 over *Horton* and *Rahman*.

Claim 2 recites the method of Claim 1 and further including the step of storing the generated value in an entry in a branch instruction queue associated with the selected group of instructions. Claim 2 has been rejected on teaching in *Horton* discussed above generally discussing branch prediction techniques and loading a predetermined predictor, and which plainly do not disclose the aforementioned limitations of claim 1. (Paper No. 3, page 4) (citing *Horton*, Abstract and col. 2, line 43 through col. 3, line 14). The Examiner also relies on teaching in *Horton* discussing a branch history table indexed by the contents of the branch history register. (Paper No. 3, page 4) (citing *Horton*, col. 9, line 66 through col. 10, line 2). By the plain terms of the teaching, *Horton* does not disclose the limitation of claim 2. A branch history table is not a branch instruction queue. Consequently, for at least the aforesaid reasons, neither *Horton* nor *Rahman* alone or in combination teach or suggest the limitations of claim 2. No further motivation for combining references has been provided beyond that asserted with respect to claim 1.

Thus, for at least the aforesaid reasons, a *prima facie* showing of obviousness has not been made for claim 2. Therefore, claim 2 is allowable under 35 U.S.C. § 103 over *Horton* and *Rahman*.

Claim 3 recites the method of Claim 2 and further including the step of correcting the generated vector upon a misprediction including the substeps of:

retrieving a selected number of bits of the vector stored from the branch instruction queue into the shift register; and shifting an updated history bit into the shift register. The Examiner asserts that *Horton* teaches the limitations of claim 3 in disclosing loading the contents of the check point register in the branch history shift register (BHSR), and shifting a bit into the BHSR corresponding to the actual resolution of a mispredicted branch. (Paper No. 3, page 4) (citing *Horton*, col. 9, lines 20-65.) The difference between the invention of claim 3 and the teachings of *Horton* include at least *Horton's* not disclosing or suggesting a branch instruction queue (BIQ) as recited in claim 3 (as well as claim 2 from which claim 3 depends), nor retrieving a selected number of bits of the vector stored in the BIQ. Consequently, for at least the aforesaid reasons, neither *Horton* nor *Rahman* alone or in combination teach or suggest the limitations of claim 3. No further motivation for combining references has been provided beyond that asserted with respect to claim 1.

Thus, for at least the aforesaid reasons, a *prima facie* showing of obviousness has not been made for claim 3. Therefore, claim 3 is allowable under 35 U.S.C. § 103 over *Horton* and *Rahman*.

Claim 4 recites the method of Claim 1 wherein the first value comprises a logic 1 and the second value is a logic 0. While the Applicant does not dispute that *Horton* teaches logic 1 and logic 0, *Horton* does not teach the first and second values as recited in claim 1. Thus, it necessarily does not teach the logic 1 and logic 0 of claim 4. Consequently, for at least the aforesaid reasons, neither *Horton* nor *Rahman* alone or in combination teach or suggest the limitations of claim 4. No further motivation for combining references has been provided beyond that asserted with respect to claim 4.

Thus, for at least the aforesaid reasons, a *prima facie* showing of obviousness has not been made for claim 4. Therefore, claim 4 is allowable under 35 U.S.C. § 103 over *Horton* and *Rahman*.

Claim 5 recites the method of Claim 1 wherein the selected group of instructions comprises eight instructions. The examiner asserts that *Rahman*, by

stating that "one or more instructions are fetched," discloses eight instructions are fetched because one or more includes eight. (Paper No. 3, pages 4-5.) This is not a correct conclusion. The generic does not disclose the particular, simply because it might include it. For example, recall, that all of the limitations in a claim must be considered in judging the patentability of the claim. MPEP § 2143.03. The Examiner's position excludes, at least, the words "eight instructions." Consequently, for at least the aforesaid reasons, neither *Horton* nor *Rahman* alone or in combination teach or suggest the limitations of claim 5.

The Examiner also recites the same motivation for combining references as has been asserted with respect to claim 1. (Paper No. 3, page 5.)

Thus, for at least the aforesaid reasons, a *prima facie* showing of obviousness has not been made for claim 5. Therefore, claim 5 is allowable under 35 U.S.C. § 103 over *Horton* and *Rahman*.

Claim 6 is directed to a method of performing branch predictions including the steps of:

indexing a branch history table using a first global history vector associated with a first fetch group of instructions during a first fetch cycle to retrieve a first prediction value;

generating a second global history vector associated with a second fetch group of instructions including the substeps of:

retaining the first vector when the first fetch group does not contain at least one branch instruction;

appending a bit of a first value to the first vector when the first fetch group has at least one branch instruction predicted to be a branch taken; and

appending a bit of a second value to the first vector when the first group contains at least one branch instruction and contains no branch instructions predicted to be a branch taken; and

indexing the branch history table using the second global history vector during a second fetch cycle to retrieve a second branch prediction value.

With respect to the limitation in claim 6 of indexing a branch history table using a first global history vector (GHV) associated with a first fetch group of instructions... , the Examiner asserts the same general discussion of branch prediction mechanisms in *Horton* discussed above in conjunction with claim 1. (*See* Paper No. 3, page 5) (citing *Horton*, Abstract and col. 2, line 43 through col. 3, line 14). Plainly, there is no teaching of this limitation therein. Indeed, the Examiner admits that *Horton* does not teach a fetching a group of instructions, and therefore it necessarily cannot teach using a GHV associated with a first fetch group because, admittedly, no such group is taught in *Horton*.

With respect to the limitation in claim 6 reciting the step of generating a second GHV associated with a second fetch group... , the Examiner asserts the same teachings in *Horton* as relied upon in rejecting claim 1. (*See* Paper No. 3, page 5) (citing *Horton*, col. 8, lines 43-55; Abstract; col. 2, line 43 through col. 3, line 14; col. 8, line 63 through col. 9, line 16; FIGURES 2-4). As discussed above, the plain teachings of *Horton* do not disclose or suggest these limitations of claim 6. Moreover, *Horton* admittedly fails to teach fetching a group of instructions, and therefore it necessarily cannot teach generating a GHV associated with a second fetch group because, admittedly, no such group of instructions is taught in *Horton*. (*See*, Paper No. 3, page 6.) Moreover, as the Applicant has discussed hereinabove, the teachings in *Horton* do not disclose, at least, respectively shifting first and second values into a history shift register when the selected group contains a branch instruction that is predicted taken, and when the selected group contains a branch instruction not including a branch instruction predicted as taken.

Consequently, for at least the aforesaid reasons, neither *Horton* nor *Rahman* alone or in combination teach or suggest the limitations of claim 6. No further motivation for combining references has been provided beyond that asserted with respect to claim 1. (*See* Paper No. 3, page 6.)

Thus, for at least the aforesaid reasons, a *prima facie* showing of obviousness has not been made for claim 6. Therefore, claim 6 is allowable under 35 U.S.C. § 103

over *Horton* and *Rahman*.

Claim 7 recites the method of Claim 6 and further including the step of storing the first and second vectors in an entry of a branch history queue associated with the first fetch group. Claim 7 has been rejected on teaching in *Horton* discussing, generally, branch prediction mechanisms, discussed above. (Paper No. 3, page 4) (citing *Horton*, Abstract and col. 2, line 43 through col. 3, line 14). The Examiner further relies on teaching that discusses indexing into a branch history table containing two-bit counters using the BHSR, and using the most-significant bit as a predictor. (Paper No. 3, page 4) (citing *Horton*, col. 9, line 66 through col. 10, line 20, and FIGURES 2-4). Plainly, this does not disclose storing first and second vectors in a branch history queue. Further, *Horton* admittedly fails to teach fetching a group of instructions, and thus, cannot teach a first fetch group. For the reasons discussed above, *Rahman* does not cure the deficiencies in *Horton*.

Consequently, for at least the aforesaid reasons, neither *Horton* nor *Rahman* alone or in combination teach or suggest the limitations of claim 7. No further motivation for combining references has been provided beyond that asserted with respect to claim 1. (*See* Paper No. 3, page 6.)

Thus, for at least the aforesaid reasons, a *prima facie* showing of obviousness has not been made for claim 7. Therefore, claim 7 is allowable under 35 U.S.C. § 103 over *Horton* and *Rahman*.

Claim 8 recites the method of Claim 7 and further including the steps of detecting a branch misprediction based on the first prediction value, retrieving the first and second vectors from the branch history queue, indexing the branch history table (BHT) using the first vector to correct the first prediction value, and appending a corrected bit to the second vector to generate a corrected branch history vector. Claim 8 has been rejected on the same teaching in *Horton* relied upon in rejecting, *inter alia*, claim 7. (*See* Paper No. 3, page 7.) Plainly, there is no teaching in *Horton* disclosing, at least, retrieving first and second vectors from a branch history queue.

Neither is there teaching disclosing, at least, indexing into the BHT using the first vector to correct the first prediction value, and appending a corrected bit to the second vector to generate a corrected branch history vector. In contrast, *Horton*, teaches a single branch history shift register, and shifting a value into that register. (*Horton*, FIGURES 2-4, and associated written description.)

Consequently, for at least the aforesaid reasons, neither *Horton* nor *Rahman* alone or in combination teach or suggest the limitations of claim 8. No further motivation for combining references has been provided beyond that asserted with respect to claim 1. (*See* Paper No. 3, page 7.)

Thus, for at least the aforesaid reasons, a *prima facie* showing of obviousness has not been made for claim 8. Therefore, claim 8 is allowable under 35 U.S.C. § 103 over *Horton* and *Rahman*.

Claim 9 recites the method of Claim 7 wherein the first fetch cycle precedes the second fetch cycle by three fetch cycles. The Examiner asserts that *Horton* teaches that a pipeline requires a certain number of cycles before another instruction is fetched for the pipeline. (Paper No. 3, page 7) (citing *Horton*, col. 1, line 49 through col. 2, line 32). Although the Applicant does not necessarily agree with that interpretation of the referred-to disclosure, there is no dispute that *Horton* does not teach or suggest a first fetch cycle preceding the second fetch cycle, as recited in claim 9, by three fetch cycles.

Consequently, for at least the aforesaid reasons, neither *Horton* nor *Rahman* alone or in combination teach or suggest the limitations of claim 9. No further motivation for combining references has been provided beyond that asserted with respect to claim 1. (*See* Paper No. 3, page 7.)

Thus, for at least the aforesaid reasons, a *prima facie* showing of obviousness has not been made for claim 9. Therefore, claim 9 is allowable under 35 U.S.C. § 103 over *Horton* and *Rahman*.

Claim 10 recites the method of Claim 7 wherein the steps of indexing

comprises the step of gating the vector with selected bits of a current instruction address. Claim 11 further recites the method of Claim 10 wherein the steps of gating comprise the steps of performing XOR operations. The Applicant does not dispute that *Horton* teaches XORing a branch history vector to index into a history table. However, a claimed invention is not a set of disembodied elements. The claimed invention as a whole must be considered in an obviousness rejection. MPEP § 2141.01. Because the claims from which claims 10 and 11 respectively depend have not been shown to be *prima facie* obvious, claims 10 and 11 are necessarily nonobvious.

Consequently, for at least the aforesaid reasons, neither *Horton* nor *Rahman* alone or in combination teach or suggest the limitations of claim 10 and 11. No further motivation for combining references has been provided beyond that asserted with respect to claim 1. (*See* Paper No. 3, page 8.)

Thus, for at least the aforesaid reasons, a *prima facie* showing of obviousness has not been made for claims 10 and 11. Therefore, claims 10 and 11 are allowable under 35 U.S.C. § 103 over *Horton* and *Rahman*.

Claim 12 recites the method of Claim 8 wherein the substeps of appending comprise the substeps of shifting a bit into a shift register storing the second vector. Claim 12 has been rewritten hereinabove to correct a typographical error referring to the first rather than second vector, as stated in claim 8. Claim 12 has been rejected on teaching that states that, in response to a misprediction, after the prior branch history is loaded into the BHSR, a one bit value corresponding to the mispredicted branch is shifted into the shift register. (*See* Paper No. 3, page 8) (citing *Horton*, col. 9, lines 20-65). As previously discussed, *Horton* does not disclose or suggest a first and second history vector, and the teachings relied upon by the Examiner are not to the contrary. Thus, it cannot disclose shifting a into the shift register storing the second vector.

Consequently, for at least the aforesaid reasons, neither *Horton* nor *Rahman*

alone or in combination teach or suggest the limitations of claim 12. No further motivation for combining references has been provided beyond that asserted with respect to claim 1. (*See* Paper No. 3, page 8.)

Thus, for at least the aforesaid reasons, a *prima facie* showing of obviousness has not been made for claim 12. Therefore, claim 12 is allowable under 35 U.S.C. § 103 over *Horton* and *Rahman*.

Claim 13 is directed to branch processing circuitry. The circuitry includes:

a shift register for storing a global history vector;

control circuitry for selectively updating a first global history vector stored in the shift register operable to:

determine if a selected group of instructions contains a branch instruction;

maintain the first global history vector in the shift register when the selected group does not contain a branch instruction;

shift a first value into the shift register to generate a second vector if the selected group contains a branch instruction and the branch instruction is predicted as a branch taken; and

shifting a second value into the shift register to generate a second vector when the selected group contains a branch instruction and does not contain a branch instruction predicted as a branch taken.

With respect to the limitation directed to the control circuitry operable to determine if a selected group of instructions contains a branch instruction, the Examiner asserts that *Horton* teaches control circuitry for determining if a branch is present. (Paper No. 3, page 8) (citing *Horton*, col. 8, lines 34-49). This is different that the limitation in claim 13, which does not recite circuitry operable to determine if a branch is present. All words in a claim must be considered when judging the patentability of the claim. MPEP § 2143.03.

With respect to the limitations drawn to circuitry operable for maintaining a first global vector... , and respectively shifting a first value... and a second value...

, the Examiner relies on the same teaching in *Horton* referred to in rejecting, *inter alia*, claim 1. These teachings have been discussed hereinabove, and by their plain terms do not disclose the circuitry as recited in claim 13. Further, the Examiner admits that *Horton* does not teach fetching a selected group of instructions. Also, as discussed hereinabove, the teaching of *Rahman* does not cure the deficiency in *Horton* for at least the reasons that there is nothing in *Rahman* that discloses or suggests, for example, determining if a selected group of instructions contains a branch instruction, or shifting a first value or second into the shift register when the selected group respectively contains a branch instruction predicted taken, and does not contain a branch predicted taken.

Consequently, for at least the aforesaid reasons, neither *Horton* nor *Rahman* alone or in combination teach or suggest the limitations of claim 13. No further motivation for combining references has been provided beyond that asserted with respect to claim 1. (*See* Paper No. 3, page 9.)

Thus, for at least the aforesaid reasons, a *prima facie* showing of obviousness has not been made for claim 13. Therefore, claim 13 is allowable under 35 U.S.C. § 103 over *Horton* and *Rahman*.

Claim 14 recites the branch processing circuitry of Claim 13 and further including a branch history table and circuitry for generating an index to an entry in the branch history table using selected bits from a current address and selected bits of the first vector to retrieve a prediction value stored therein. The Applicant does not dispute that *Horton* teaches generating an index to an entry in the branch history table using selected bits from a current address and selected bits of the first vector. However, a claimed invention is not a set of disembodied elements. The claimed invention as a whole must be considered in an obviousness rejection. MPEP § 2141.01. Because the claims from which claim 14 depends have not been shown to be *prima facie* obvious, claim 14 is necessarily nonobvious.

Claim 15 recites the branch processing circuitry of Claim 14 and further including circuitry for updating the second vector when the prediction value results in

a misprediction. This circuitry includes: a queue for storing the first and the second vectors, circuitry for accessing the vectors from the queue, circuitry for indexing the branch history table with the first vector and updating a corresponding entry with a corrected prediction value, circuitry for updating a vector in the shift register with the second vector, and circuitry for shifting the corrected prediction value into the shift register. As discussed hereinabove in conjunction with, *inter alia*, claim 13, *Horton* does not teach the circuitry operable for generating the first and second vectors as recited in claim 15. Thus, necessarily, *Horton* cannot teach the queue for storing the first and second vectors, as these vectors do not exist in *Horton.* Although, the Applicant does not necessarily agree with the assertion that registers act like queues, *Horton* does not teach a queue for storing the first and second vectors, as recited in claim 15. In particular, the BHSR and checkpoint register in *Horton* do not store the first and second vectors of claim 15.

Consequently, for at least the aforesaid reasons, neither *Horton* nor *Rahman* alone or in combination teach or suggest the limitations of claim 15. No further motivation for combining references has been provided beyond that asserted with respect to claim 1. (*See* Paper No. 3, page 10.)

Thus, for at least the aforesaid reasons, a *prima facie* showing of obviousness has not been made for claim 15. Therefore, claim 15 is allowable under 35 U.S.C. § 103 over *Horton* and *Rahman*.

Claim 16 recites the branch processing circuitry of Claim 13 wherein the branch processing circuitry forms a portion of a single-chip microprocessor. The Applicant does not dispute that *Horton* teaches a single-chip microprocessor. However, a claimed invention is not a set of disembodied elements. The claimed invention as a whole must be considered in an obviousness rejection. MPEP § 2141.01. Because the claim from which 16 depends has not been shown to be *prima facie* obvious, claim 16 is necessarily nonobvious.

Consequently, for at least the aforesaid reasons, neither *Horton* nor *Rahman*

alone or in combination teach or suggest the limitations of claim 16. No further motivation for combining references has been provided beyond that asserted with respect to claim 1. (*See* Paper No. 3, page 10.)

Thus, a *prima facie* showing of obviousness has not been made for claim 16. Therefore, claim 16 is allowable under 35 U.S.C. § 103 over *Horton* and *Rahman*.

Claim 17 is directed to a processing system. The system includes a microprocessor. The microprocessor includes a branch history table for storing branch prediction values, a global history shift register for storing a global branch history vector, logic for generating an index to the branch history table and accessing prediction values stored therein using selected bits of a the branch history vector stored in the shift register, and control circuitry for updating the global branch history vector stored in the shift register and operable to retain a current vector stored in the shift register when a selected fetch group does not contain at least one branch instruction; shift a bit of a first value into the shift register to generate an updated vector when the selected fetch group has at least one branch instruction predicted to be a branch taken; and shift a bit of a second value into the shift register when the selected fetch group contains at least one branch instruction and contains no branch instructions predicted to be a branch taken. With respect to the limitation in claim 15 directed to control circuitry for updating the GHV including control circuitry operable to operable for maintaining a first global vector... , and respectively shifting a first value... and a second value... , the Examiner relies on the same teaching in *Horton* referred to in rejecting, *inter alia*, claim 1. (*See* Paper No. 3, pages 11-12.) These teachings have been discussed hereinabove, and by their plain terms do not disclose the circuitry as recited in claim 13. Further, the Examiner admits that *Horton* does not teach fetching a selected group of instructions. Also, as discussed hereinabove, the teaching of *Rahman* does not cure the deficiency in *Horton* for at least the reasons that there is nothing in *Rahman* that discloses or suggests, for example, determining if a selected group of instructions contains a branch instruction, or shifting a first value or second into the shift register when the selected group respectively contains a

branch instruction predicted taken, and does not contain a branch predicted taken.

Consequently, for at least the aforesaid reasons, neither *Horton* nor *Rahman* alone or in combination teach or suggest the limitations of claim 17. No further motivation for combining references has been provided beyond that asserted with respect to claim 1. (*See* Paper No. 3, page 12.)

Thus, a *prima facie* showing of obviousness has not been made for claim 17. Therefore, claim 17 is allowable under 35 U.S.C. § 103 over *Horton* and *Rahman*.

Claim 18 recites the processing system of Claim 17 wherein the microprocessor further includes a branch instruction queue having a plurality of entries each associated with a fetch group for storing at least first and second corresponding global history vectors, circuitry for detecting a misprediction associated with a the prediction value retrieved from the branch history table and corresponding to the first global history vector in the branch instruction queue, circuitry for retrieving the first vector from the branch instruction queue and accessing a corresponding entry in the branch history table to correct the prediction value stored therein, and circuitry for retrieving and modifying the second vector to generate a corrected vector in the shift register.

With respect to the branch instruction queue having a plurality of entries each associated with a fetch group for storing the first and second vectors... , the Examiner asserts that *Horton* teaches a BIQ having a plurality of entries for storing at least a first and second corresponding global history vector. (Paper No. 3, page 13.) As an initial matter, this does not address the limitation of claim 18. Claim 18 does not only recite a BIQ having a plurality of entries for storing at least a first and second corresponding global history vector. All words in the claim must be considered when considering the patentability of the claim. MPEP §2143.03. Moreover, the Examiner admits that *Horton* does not teach fetch groups. (Paper No. 3, page 13.) Thus, logically, *Horton* cannot teach the BIQ as recited claim 18 because *Horton* necessarily cannot teach a plurality of entries each associated with a fetch group.

As previously discussed in conjunction with, *inter alia*, claim 1, the teaching in *Rahman* asserted to disclose fetch groups does not cure the deficiencies in *Horton*. Although the Examiner admits that Horton does not teach fetch groups, no teaching with respect to a BIQ having a plurality entries each associated with a fetch group. Thus the alleged teaching in *Rahman* that *Rahman* teaches fetching a group of instructions does not address the limitation of claim 18. Indeed, the Examiner does not assert that the references disclose a BIQ having a plurality entries each associated with a fetch group.

With respect to the motivation for combining the references, the motivation is the same as asserted with respect to claim 1. (*See* Paper No. 3, page 13.) It is inadequate to support a *prima facie* showing of obviousness for the reasons discussed hereinabove.

Consequently, for at least the aforesaid reasons, neither *Horton* nor *Rahman* alone or in combination teach or suggest the limitations of claim 18. No further motivation for combining references has been provided beyond that asserted with respect to claim 1. (*See* Paper No. 3, page 13.)

Thus, a *prima facie* showing of obviousness has not been made for claim 18. Therefore, claim 18 is allowable under 35 U.S.C. § 103 over *Horton* and *Rahman*.

Claim 19 recites the processing system of Claim 17 wherein the processing system further includes a system memory coupled to the microprocessor by a bus. A claimed invention is not a set of disembodied elements. The claimed invention as a whole must be considered in an obviousness rejection. MPEP § 2141.01. Because the claims from which claim 19 depends have not been shown to be *prima facie* obvious, claim 19 is necessarily nonobvious.

Claim 20 recites the processing system of Claim 17 wherein the fetch group comprises eight instructions. The examiner asserts that *Rahman*, by stating that "one or more instructions are fetched," discloses eight instructions are fetched because one or more includes eight. (Paper No. 3, page 14.) This is not a correct conclusion. The

generic does not disclose the particular, simply because it might include it. For example, recall, that all of the limitations in a claim must be considered in judging the patentability of the claim. MPEP § 2143.03. The Examiner's position excludes, at least, the words "eight instructions." Consequently, for at least the aforesaid reasons, neither *Horton* nor *Rahman* alone or in combination teach or suggest the limitations of claim 20.

The Examiner also recites the same motivation for combining references as has been asserted with respect to claim 1. (*See* Paper No. 3, page 14.)

Thus, for at least the aforesaid reasons, a *prima facie* showing of obviousness has not been made for claim 20. Therefore, claim 20 is allowable under 35 U.S.C. § 103 over *Horton* and *Rahman*.

As a result of the foregoing, Applicant respectfully asserts that there are numerous claim limitations not taught or suggested in the cited prior art, and thus the examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-20 in view of the cited prior art.

III. CONCLUSION

As a result of the foregoing, it is asserted by Applicant that claims 1-20 in the Application are in condition for allowance, and Applicant respectfully requests an allowance of such claims. Applicant respectfully requests that the Examiner call Applicant's attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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